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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
NGUYEN, STEVE N	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,793	ZORIAN ET AL.	
	Examiner	Art Unit	
	Steve Nguyen	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-19,21-23 and 25-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,4,12,27,29,30 and 32* is/are allowed.

6)☒ Claim(s) *2,6,7,9-11,13,15-19,21-23,25,26,28,31 and 33-38* is/are rejected.

7)☒ Claim(s) *5,6,8 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/20/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13, 15-19, 21-23, and 25-38 are currently pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/20/2007 has been entered.

Allowable Subject Matter

3. Claims 1, 3, 4, 12, 27, 29, 30, and 32 are allowed. Claims 2, 6-11, 13, 15-19, 21, and 28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: the present invention is directed to generating and storing a concatenated compressed repair signature in a fuse box. The prior art teach various methods of generating a compressed repair signature. Anand et al (US 6577156) and Ouellette et al ("Shared fuse macro for multiple embedded memory devices with redundancy") teach

compressing repair data to be stored in a fuse box for a plurality of memories by using a run-length compression algorithm. The stored concatenated repair data is then shifted in a scan chain to the memories. Ito (US 6804156) teaches a fuse box for storing compressed repair data for a plurality of memories wherein the compression algorithm comprises operands that generate repair data for a particular memory identified by an ID operand and indicates a programmed number of non-defective devices to be skipped, thereby reducing the number of fuses required for storing data.

None of the prior art of record teach or suggest the feature that the concatenated repair signature comprises a string of bits arranged as a plurality of fields, one field for each of the memories, wherein for each memory having one or more defective memory cells detected during fault testing, the field consists of a single bit that identifies the memory followed by a plurality of bits being compressed, repair signature data for the memory; and for each memory with no defective memory cells, the field consists of a single bit that identifies the memory. The prior art are not concerned with the concatenated repair signature being arranged as a plurality of fields, one field for each of the memories; nor do they teach the field having a single bit that identifies each memory.

Drawings

4. The drawings are objected to because:

- they failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: fuse box 214 referenced for example on pages 10-12.
- "redundant components 204" mentioned on page 11, paragraph 19 shows an I/O circuit 204 in Fig. 2.
- "memory 332" referenced on page 12, paragraph 21 should be memory 330.
- "reconfiguration data engine 610" referenced on page 24, paragraph 47 shows a "Self Test and Repair Processor" 610 in Fig. 6.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 5, 6, 8, and 22 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s)

in proper dependent form, or rewrite the claim(s) in independent form. The limitations of claim 5 are inherently present in the parent claim. Claims 6 and 8 repeat what was already recited in claim 1.

Claim 22 recites, "wherein the concatenated repair signature that comprises a string of bits". The word "that" should be deleted to correct grammatical reasons.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 33-38 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 33-38 are directed to a "machine readable medium that stores data and executable instructions representing an integrated circuit". Referring to page 28 of the specification, a machine readable medium could embody carrier waves, infrared signals, or digital signals. Signals per se are not statutory subject matter.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, 6, 7, 9-11, 13, 15-19, 21, 28, 31 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites that "the repair data is a fuse box located external to the two or more memories". It is unclear how data could be a fuse box because data is not hardware. Applicant may have intended "repair data container". However, claim 1 requires that a repair data container is "on-chip with the two or more memories". Therefore a fuse box "external to the two or more memories" contradicts claim 1.

Claim 6 recites, "the processor further includes logic configured to compress an amount of bits making up the actual repair signature". The claim is incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are the relationship between an actual repair signature and a concatenated repair signature. It is unclear whether the compressed repair signature of claim 1 is the same as an actual repair signature. Claim 7 is similarly rejected.

Based on Applicant's disclosure, a compressed repair signature is an actual repair signature and therefore claim 6 is repeating what was recited in claim 1 and fails to further limit the subject matter of a previous claim.

Claim 9 is rejected for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are the relationship between the recited actual repair signature and dummy repair signature to the concatenated repair signature recited in claim 1. It is assumed that an actual repair

signature is a "a plurality of bits being compressed, repair signature data for the memory". However, it is unclear what dummy repair signatures are because claim 1 recites that for each memory with no defective cells, the field **consists of a single bit** that identifies the memory. Claims 28 and 31 are similarly rejected.

Claim 10 recites, "wherein the repair data container stores indicator bits for each memory sharing that repair data container". It is unclear what "that repair container" is referring to. The phrase "that repair container" implies that there are multiple repair containers.

Claim 11 recites, "wherein the fuse box has a dedicated field for each memory sharing that fuse box". It is unclear what "that fuse box" is referring to. The phrase "that fuse box" implies that there are multiple fuse boxes.

Claim 13 recites "compression/decompression logic around the repair container". It is unclear whether compression/decompression logic is compression logic or decompression logic; or whether it is compression logic and decompression logic. Furthermore, the term "around" is a relative term which renders the claim indefinite. The term "around" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear what distance the compression/decompression logic must be from the repair data container in order to be considered to be "around" the repair data container.

Claim 15 recites, "two or more processors including the first processor and a second processor". The closed-ended term "including" implies that there are no

processors other than the first processor and the second processor. Therefore the recitation "two or more processors" is unclear. Claim 15 further recites, "coupled to one or more memories". It is unclear whether the "one or more memories" are the same memories in claim 1. Claim 21 is similarly rejected.

Claim 16 recites, "to generate an augmented repair signature". It is unclear what element is augmented to the repair signature.

Claim 17 recites, "wherein the repair data container also stores dummy repair signatures for each memory with no defective memory cells". However, parent claim 16 contradictorily recites that for each memory with no defective cells the field **consists of only** one or more bits that identify the memory. Claim 19 inherits the limitations of claim 17 and is similarly rejected.

Claim 18 recites, "wherein the processor also contains redundancy allocation logic and is coupled to the repair data container". It is unclear whether the processor is coupled to the repair data container; or whether the redundancy allocation logic is coupled to the repair data container.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 22, 23, 25, 26, and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand.

As per claim 22:

Anand teaches an apparatus, comprising: a fuse box to store a concatenated repair signature (Fig. 1, element 11). Not explicitly disclosed by Anand is a first processor containing logic configured to test and repair two or more memories connected to that first processor; and a second processor containing logic configured to test and repair two or more memories connected to that second processor.

However, Anand teaches an integrated circuit for testing and repairing at least two memories connected thereto (Fig. 1, element 10). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement a second processor along with a first processor to test and repair respective memories since it is suggested by Anand in col. 3, line 67-col. 4, line 2.

Regarding the newly amended limitations of claim 22, it is noted that the specific features recited are intended use, and do not limit the apparatus claimed to any specific structure. Language that suggests or makes optional but does not require steps to be

performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. See MPEP 2106. In this case, "a fuse box to store a concatenated repair signature..." only suggests that the fuse box be used to store the concatenated repair signature, but does not limit the structure of the fuse box in the apparatus. Any conventional fuse box capable of storing data could store the concatenated repair signature.

As per claim 23:

Anand teaches the apparatus of claim 22, wherein the first processor contains logic configured to decompress an amount of bits making up the concatenated repair signature (Fig. 1, element 14).

As per claim 25:

Anand teaches the apparatus of claim 22, wherein the fuse box is located external to the memories (see Fig. 1).

As per claim 26:

Anand teaches the apparatus of claim 22, wherein the processors and the fuse box are embedded on a single chip (see Fig. 1).

As per claim 33:

Anand teaches a machine readable medium that stores data representing an integrated circuit, comprising:

- a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor (Fig. 1, element 11).

Not explicitly disclosed by Anand is a first processor containing logic configured to test and repair two or more memories connected to that first processor; and a second processor containing logic configured to test and repair two or more memories connected to that second processor. However, Anand teaches that an integrated circuit for testing and repairing at least two memories connected thereto (Fig. 1, element 10).

However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement a second processor along with a first processor to test and repair respective memories since it is suggested by Anand in col. 3, line 67-col. 4, line 2.

9. Claim 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand in view of Rona (US Pat. 5,350,940).

As per claim 34:

Anand teaches the machine-readable medium of claim 32 above. Not explicitly disclosed by Anand is wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the fuse box and the processors. However, Rona teaches fabrication of semiconductors using lithographic masks (col. 8, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lithographic mask. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made,

because one of ordinary skill in the art would have recognized that fabrication using lithographic masks is well known (col. 8, lines 35-38).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Ito (US 6804156), directed to a fuse box for storing compressed repair data for a plurality of memories wherein the compression algorithm comprises operands that generate repair data for a particular memory identified by an ID operand and indicates a programmed number of non-defective devices to be skipped.
- Adams et al (US Pat Pub. 2004/0153900), directed to a method and system for repairing memory using compressed data stored in a fuse macro.
- Vollrath (US 5831917), directed to reducing the area required in a fuse array by sharing fuses corresponding to common high-order address bits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2117

GUY LAMARRE
PRIMARY EXAMINER